REMARKS

Applicant respectfully requests further examination and reconsideration in view of the instant amendment and response. Claims 1-14 remain pending in the case. Claims 1-3 and 5-9 have been amended herein. Claims 10-14 are new. No new matter has been added.

CLAIM OBJECTIONS

Claims 1-3, 5, and 6-9 are objected to because of informalities. Appropriate amendments have been made to correct the informalities. Applicants request review and approval of these claim amendments.

CLAIM REJECTIONS
35 U.S.C. §102
Claims 1-9

Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. 5,386,563 to Thomas, deceased, hereafter referred to as Thomas. Applicant has reviewed the cited reference and respectfully submit that the embodiments of the present invention as recited in Claims 1-9 and new Claims 10-14 are not anticipated or rendered obvious by Thomas for the following reasons.

Applicant respectfully directs the Examiner to amended independent Claim 1, which recites that an embodiment of the present invention is directed to:

A method for ~~resolving~~ processing nested faults ~~including the steps of~~ comprising:

determining whether a fault is a first level fault;

responding to a determination of a first level fault with a first fault handler ~~by~~ and saving a first amount of state sufficient to handle a first level fault; and

responding to a determination of a nested fault with a second fault handler and ~~by~~ saving an additional amount of state before handling the nested fault, wherein said second fault handler supercedes said first fault handler and processes said first level fault and said nested fault.

Amended Independent Claim 5 recites similar limitations. Claims 2-4 that depend from independent Claim 1, Claims 6-10 that depend on independent Claim 5, and new Claims 10-14 provide further recitations of the features of the embodiments of the present invention.

Thomas and the claimed invention are very different. Thomas purports to teach a data processing apparatus and method in which a CPU is operable in either a main processing mode or an exception mode (abstract). Thomas also purports to teach a plurality of processing modes wherein each processing mode has its own exception data registers (abstract). However, Thomas fails to teach or suggest a plurality of fault handlers wherein said second fault handler supercedes said first fault handler and processes said first level fault and said nested fault, as claimed. Therefore, the embodiment of Claim 1, including this limitation, is not taught or rendered obvious by Thomas.

In fact, Thomas actually teaches away from the claimed limitations of the present invention by teaching a first fault handler for processing a first fault and a second fault handler for processing a nested fault wherein the second fault handler interrupts the first fault handler to process the nested fault and then the first fault handler processes the first fault after the second fault handler has finished (Figure 4). Specifically, in Column 7 lines 62-68, Thomas states "in combination with the fact that the contents of the R15pc are restored to that which they had when the SVC32 mode was exited, then the SVC32 mode processing will resume at step 78 at substantially the exact point at which it was exited." Thomas clearly uses one fault handler to process a first fault and a second fault handler to process a nested fault. The second fault handler processes the nested fault and then the first fault handler resumes processing of the first fault at the point which the second fault handler interrupted. This is very different from the present invention that uses a second fault handler to process both the first fault and the nested fault. This allows a less complex fault handler to process a first level fault and a more complex fault handler to process a nested fault in addition to a first level fault resulting in more efficient fault handling.

For the foregoing rational, Applicant respectfully asserts that Claim 1 is not anticipated or rendered obvious by Thomas. As such, allowance of Claims 1-14 is earnestly solicited.

CLAIMS 1 and 5

Claims 1 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Applicant's History of the Prior Art. The rejection is respectfully traversed for the foregoing rational.

The Office Action cites "such hardware is able to handle first level faults since the instruction at which the fault occurred is retained, by the processor but is not capable of handling nested faults by itself" (paragraph 11). However, Applicant's History of the Prior Art teaches away from the claimed invention by stating that "hardware does not save state on each fault." This is very different from the claimed limitations of the embodiments of the present invention. Claim 1 includes the limitation of saving a first amount of state sufficient to handle a first level fault and saving an additional amount of state before handling the nested fault. It is appreciated that Claim 1, including this limitation saves state for each fault.

Furthermore, Applicant's History of the Prior Art fails to teach or suggest wherein said second fault handler supercedes said first fault handler and processes said first level fault and said nested fault, as claimed. Claim 1, including this limitation, is not taught or rendered obvious by Applicant's History of the Prior Art.

For the foregoing rational, Claim 1 is not anticipated by Applicant's History of the Prior Art. As such, allowance of Claims 1 and 5 is earnestly solicited.

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-9 overcome the rejections and objections of record and, therefore, allowance of Claims 1-14 is earnestly solicited.

Should the Examiner have a question regarding the instant response, the Applicants invite the Examiner to contact the Applicants' undersigned representative at the below listed telephone number.

Respectfully submitted,

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